

Amendments to the Claims

Please amend claims 1, 2, and 4 as follows:

1. (Currently Amended) A semiconductor memory, comprising:

data I/O buses;

a plurality of prefetch/preload latch circuits (PFPLL) connected in common to each of said data I/O buses, wherein there are a predetermined number of PFPLL for each data I/O bus respectively;

a half of a data path circuit corresponding to a single array block (BK1);

the half of a data path circuit further comprising a plurality of secondary sense amplifiers (SSA),

a plurality of write buffers (WB), and the PFPLL, wherein

each secondary sense amplifier supplies read data from the memory to the corresponding PFPLL;

each write buffer supplies write data received from the data I/O bus to the corresponding PFPLL,

wherein the PFPLL temporarily retain the read or write data;

a memory cell array including a plurality of bit line pairs (BL), a plurality of bit

switches (BSW) connected between said plurality of ~~latch circuits~~ bit line pairs and ~~said a plurality~~

~~of bit line pairs~~ main switches (MSW) such that main switches are connected between a plurality

of local I/O line pairs and a plurality of main I/O line pairs (MDQ), respectively,

the plurality of main switches are turned on or off simultaneously; and

the plurality of bit switches are further divided into a plurality of groups, a plurality of column

selection lines provided so as to correspond to said plurality of groups and each of which is

connected to the plurality of bit switches included in the corresponding group, and a plurality of

sense amplifiers connected to said plurality of bit line pairs;

said secondary sense amplifiers adapted to activate when enabled by a sense amplifier enable signal;

a column decoder for driving said column selection lines; and

a control enable signal which controls the column decoder so as to drive two

or more of said column selection lines in order during activation of said

secondary sense amplifiers.

2. (Currently Amended) The memory according to claim 1, wherein said memory cell array is divided into a plurality of blocks; said semiconductor memory further comprises a block selection signal for selecting said block; and said sense amplifier enable signal activates said secondary sense amplifiers in said selected block.

3. (Previously Amended) The memory according to claim 1, wherein said semiconductor memory operates in synchronization with an external clock; and said control enable signal drives said two or more of said column selection lines in order synchronously with the external clock.

4. (Currently Amended) A burst operation method for a semiconductor memory having data I/O buses, ~~a plurality of latch circuits connected in common to each of said data I/O buses, and a memory cell array, in which said memory cell array includes a plurality of bit line pairs, a plurality of bit switches connected between said plurality of latch circuits and said plurality of bit line pairs and divided into a plurality of groups, a plurality of column selection lines provided so as to correspond to said plurality of groups and each of which is connected to the plurality of bit switches included in the corresponding group, and a plurality of sense amplifiers connected to said plurality of bit line pairs,~~

a plurality of prefetch/preload latch circuits (PFPLL) connected in common to each of said data I/O buses, wherein there are a predetermined number of PFPLL for each data I/O bus respectively; a half of a data path circuit corresponding to a single array block (BK1); the half of a data path circuit further comprising a plurality of secondary sense amplifiers (SSA), a plurality of write buffers (WB), and the PFPLL, wherein each secondary sense amplifier supplies read data from the memory to the corresponding PFPLL; each write buffer supplies write data received from the data I/O bus to the corresponding PFPLL, wherein the PFPLL temporarily retain the read or write data;

a memory cell array including a plurality of bit line pairs (BL), a plurality of bit switches (BSW) connected between said plurality of bit line pairs and a plurality of main switches (MSW) such that main switches are connected between a plurality of local I/O line pairs and a plurality of main I/O line pairs (MDQ), respectively, the plurality of main switches are turned on or off simultaneously; the plurality of bit switches are further divided into a plurality of groups, a plurality of column selection lines provided so as to correspond to said plurality of groups; said secondary sense amplifiers adapted to activate when enabled by a sense amplifier enable signal;
a column decoder for driving said column selection lines; and
a control enable signal which controls the column decoder so as to drive two or more of said column selection lines in order during activation of said secondary sense amplifiers.

the burst operation method, comprising the steps of:
 activating said secondary sense amplifiers; and
 driving two or more of said column selection lines in order during activation of said secondary sense amplifiers.

5. (Original) The method according to claim 4, wherein said memory cell array is divided into a plurality of blocks; said burst operation method further comprises a step of selecting said block; and
 the sense amplifiers in the selected block are selectively activated in said sense amplifier activating step.

6. (Original) The method according to claim 4, wherein said semiconductor memory operates in synchronization with an external clock; and
 said two or more of the column selection lines are driven in order synchronously with the external clock in said column selection line driving

step.